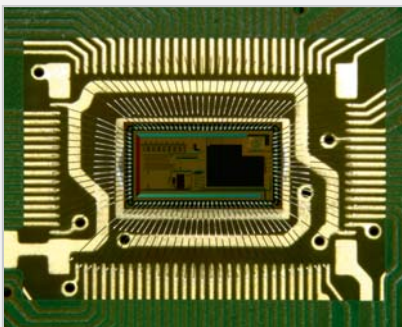


Nano-HySiF – Nano contacts for flexible electronics

Nano contacts are used to apply ultra-thin chips to flexible films like Velcro. In cooperation with our partner NanoWired, the technology is being researched and tested for applications in flexible electronic systems for medical technology.

[Nano-HySiF](#) page 2

PanaMEA – ASIC for a Miniature Pancreatic Implant



In the BMBF-funded PanaMEA project, an ASIC for a miniature pancreatic implant is developed at IMS CHIPS. A unique feature of the design is an integrated solution for FOPP (Fraction of Plateau Phase) detection of the beta-cell activity. Smart approach is adopted to keep the design overhead to a minimum, resulting in a low-power system with highly reduced data volume, which can be applied to more advanced beta-cell activity monitoring.

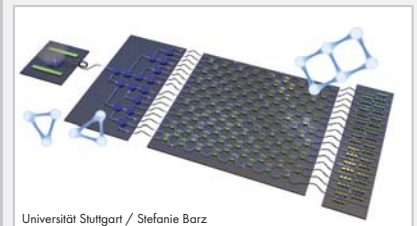
[PanaMEA](#) page 3

IMS CHIPS as alliance partner for the production of next generation integrated circuits

In order to meet the growing demand for more computing power, especially in networked devices, the technologies to manufacture high-performance chips in the 2-nm process must be developed today. The prerequisites for mass production should be in place by 2025. IMS CHIPS supports the work to establish the 2-nm node within the ECSEL project ID2PPAC.

[ID2PPAC](#) page 3

PhotonQ - Measurement-based and scalable quantum processor



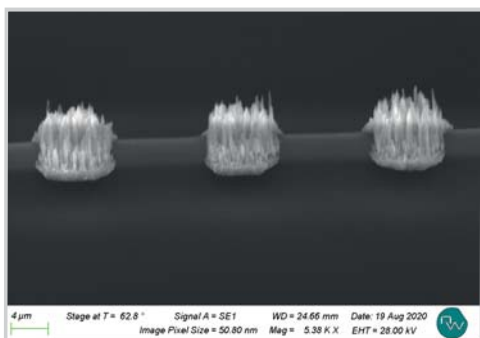
Universität Stuttgart / Stefanie Barz

In the PhotonQ project, funded by the BMBF, a measurement-based and scalable processor for a photonic quantum computer will be developed with our university partners. At the heart of the quantum processor is an integrated photonic chip, which is being researched and developed at the IMS. For this purpose, new types of phase shifters, integrated optical circuits and optical interconnect technology will be investigated.

[PhotonQ](#) page 4

New contacting technology for flexible systems

Nano contacts for reliable integration of ultra-thin silicon chips in flexible films



Flexible electronic systems are increasingly conquering market segments, particularly in the fields of medical technology and life style products, while creating a wide range of new products. The development is driven by medical applications, such as catheters, which, when equipped with sensor functions, show significant improvements in work processes and thus in operational safety and patient protection. This is only possible by integrating high-performance silicon components (sensors, ASICs and microprocessors) into the flexible film, because the required functionality cannot be achieved with thin-film components alone. At IMS, these hybrid systems-in-film (HySiF) with embedded thinned silicon chips have been researched for years. Using the patented Chip-Film Patch (CFP) technology, we have been manufacturing flexible multi-chip modules with embedded ASICs and micro controllers in combination with printed sensors and other thin-film components. The wafer-based and CMOS-compatible CFP technology facilitates chip interconnections with pad sizes < 10 μm and small pad spacings using adaptive layout processes with laser direct writing. The key factor here is reliable contacting of the various components (sensors, ICs) into the flexible system. The CFP process is similar to semiconductor processes with sputtering and etching processes as well as lithographic structuring. The Nano-HySiF project explores a different approach using nano contacts. Cooperating with the Hessen-based company NanoWired, the IMS has been working on the integration of ultra-thin silicon chips into flexible foil systems since 2021. The hair-thin metal rods can be up to a few micrometers long, depending on the application and contact size. The contact diameters that can be produced with a nano-wiring structure

range from 3 μm to several millimeters. The materials of these nano-wiring structures are usually made of copper, but can also be made of gold, silver, nickel or platinum. Once the nano-wiring structures have been created on the substrates, the user has various bonding methods at his disposal, for which NanoWired has introduced the process designations "Velcro-Welding, Velcro-Sintering, Velcro-Glueing". If there are nano contacts on both workpieces to contact, the joining process can take place at room temperature. Similar to Velcro, the nano structures form mechanical and thus also electrical connections. With modified joining parameters (temperature and pressure), systems can also be joined that have nano structures on only one side of the contact. For chip structures on rigid systems, electrical resistances of < 1 μOhm/mm² and thermal conductivities of 350 W/mK with strengths of up to 60 MPa were achieved. The contacting of thinned and thus bendable silicon chips naturally poses a special challenge to the packaging technology, but offers a variety of advantages for hybrid integration. For example, face-down mounting of chips on the prepared foil simplifies the process considerably, and time-consuming via etching processes on the embedded chips are no longer necessary. With the already proven small contact sizes and pitches < 10 μm and low temperature requirements, the nano-wired technology also enables the direct assembly of small chiplets with minimal structure sizes onto foil systems. When producing medical catheters, minimal dimensions and the size of these chiplets are also crucial. The current project is therefore using a foil with bending sensors for a catheter application to evaluate the technology. Initially, however, the partners will be working with thinned silicon chips that have a variety of

different contacts and test structures. Fig. 2 shows such contact pads on these chips

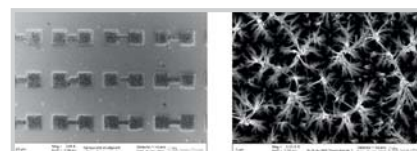


Fig. 2 Scanning electron microscope image of nano-structures on a thinned silicon chip

thinned back to 30 μm after singulation. In Fig. 3, the infrared transmitted-light image shows the connections joined to the foil

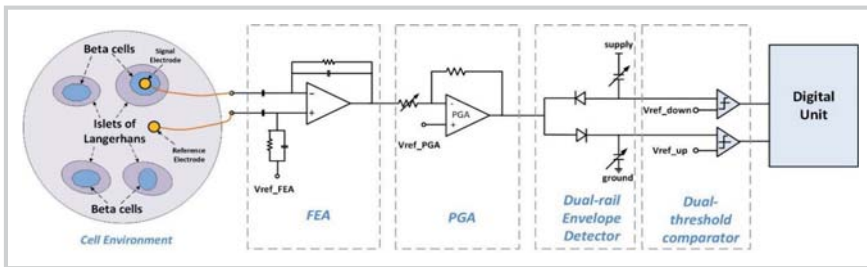


Fig. 3 Infrared image of a joined hybrid foil system with nano contacts.

carrier and thus electrically contacted connections. After complete integration into the corresponding foil systems, the process parameters as well as minimum achievable structure sizes and, above all, the reliability of the contacts under mechanical and thermal loads are determined. By the end of the project at the end of the year, a process to manufacture hybrid electronic systems with nano contacts will be available.

PanaMEA - ASIC for a Miniature Pancreatic Implant

Front-end signal processing of Beta-cell electrical activities captured by a Micro-Electrode Array (MEA)



Front-end beta-cell signal processing scheme

There are millions of people worldwide suffering from type 2 diabetes mellitus, which is caused by the body's ineffective use of insulin. The insulin is generated in the beta-cells in the pancreas. There is a direct relationship between the beta-cell's electrical activity in the form of membrane oscillatory bursts and extracellular glucose concentration. In the BMBF project "PanaMEA" (Pankreas-Implantat auf MEA-Basis, grant number 13GW0397), a miniaturized pancreatic

implant is being developed that measures this electrical activity.

The main task for IMS CHIPS is to develop a low-power front-end ASIC to do signal processing of the beta-cell signals captured by a microelectrode array (MEA). A bio-marker, the so-called Fraction of Plateau Phase (FOPP), is defined for the beta-cell signal. It is the percentage of time with beta-cell activity. A high FOPP corresponds to a high glucose level. In conventional beta-cell mon-

itoring methods, all signal details, including FOPP-irrelevant high frequency contents are recorded, and the FOPP value is calculated by postprocessing this signal. This will lead to a big data volume and results in a system with high-power consumption for data transmission and processing. Instead of recording all the signal details, we have used a very simple circuit structure, i.e., a differential envelope detector with diodes and capacitors, to filter out the high frequency contents and obtain the FOPP-relevant information. The design overhead is kept to a minimum and the data volume is highly reduced. The idea and the effectiveness of the circuits are validated by ASIC measurements. The next steps are to carry out in-vitro measurements and encapsulate the ASIC for implantation experiments.

Contact: Zili Yu • phone +49 711 21855-325 • Ziliyu@ims-chips.de

Technology development for the 2-nm node

IMS CHIPS as a joint partner in the Eysel project ID2PPAC



© spainter_vfx - stock.adobe

The ECSEL joint project ID2PPAC, funded by the European Union and the German Federal Ministry of Education and Research (BMBF) with nearly 48 million euros, will consolidate and integrate the technology solutions for the 2-nm node identified in previous work. The goal is to demonstrate that the Performance Power Area and Cost (PPAC) requirements for this new generation of leading logic technology are within reach.

To continue the so-called Moore's Law for the 2-nm node while meeting the PPAC requirements, a combination of further advances in EUV lithography & masks, 3D

device structures, materials and metrology is required. The strength of the project is based on a common pilot line and the focused commitment of the partners involved, who have exceptional expertise in key interrelated areas.

The ID2PPAC project is expected to enable IC-Fabs to perform so-called EUV-based single-print high-volume manufacturing for the 2-nm node by 2025.

To meet the ever-increasing demand for more computing power, the semiconductor industry is continuously working on technological innovations to realize this progress as predicted by Moore's Law and will continue to do so.

The project will also help build Europe's technological capability in this area, which is critical for digitization, (edge) AI and to solve national, European and global societal challenges, as well as strengthen the consortium of leading European companies and research facilities active in this field.

Institut für Mikroelektronik Stuttgart (IMS

CHIPS) will participate in the Lithography Equipment work package. A part of this work package is the development of high-precision diffractive optical elements (DOE) for surface inspection of EUV mirrors.

Contact: Julian Hartbaum • phone +49 711 21855-471 • hartbaum@ims-chips.de

PhotonQ project launched

Exploring a measurement-based and scalable quantum processor



Phase shifters for the optical gates

The idea behind quantum computers is that they are expected to one day solve problems at a high speed that are not workable for classic computer systems. However, until those computers become practical, they will have to process a significantly higher number of qubits and prove lower error rates. A joint research group around Professor Stefanie Barz of the University of Stuttgart is currently developing a photonic quantum processor, which will allow the realization of quantum algorithms with

to explore new, scalable quantum processors: Atomic and ion traps, superconductors, semiconductors or entangled photons. In the PhotonQ project, which is funded by the German Federal Ministry of Education and Research (BMBF) with around 16 million euros, the Universities of Stuttgart, Würzburg, Mainz and Ulm, the Technical University of Munich, Institut für Mikroelektronik Stuttgart and Vanguard Automation GmbH aim to develop a processor for a photonic quantum computer.

a small number of qubits and, in the long run, enable rapid scaling to qubit numbers relevant to practical applications.

A wide variety of approaches exist

At the heart of the quantum processor is an integrated photonic chip.

In PhotonQ, IMS CHIPS is researching and developing the integrated photonic chips with new types of components, such as extremely low-attenuation phase shifters (see cover image: Principle of the measurable quantum processor). In addition, an optical AVT with low transmission losses will be established.

Contact: Mathias Kaschel • phone +49 711 21855-467 • kaschel@ims-chips.de

News Flash

Best Paper Award -- For the paper: "Front-End Electronics for Beta-Cell Function Monitoring with an Integrated FOPP Detector", Dr. Zili Yu and co-authors received the First Place Best Paper Award at IEEE SENSORS.

Joint project SensIC – In this joint project, BMBF is funding the development of reliable electronic components that are integrated directly into machine components and determine safety-relevant sensor data there. IMS CHIPS supports KIT in a development contract with hybrid foil systems and integration technologies. For further information, please visit <https://www.nanomat.de/sensIC.php>.

Nanopatterning Cluster+ – Nanopatterning Cluster+ - IMS CHIPS receives a grant of 6.4 million euro for the project Nanopatterning Cluster+ and 1.98 million euro for the project Nanopatterning Cluster+ Phase 2 from the Ministerium für Wirtschaft, Arbeit und Tourismus Baden-Württemberg within the framework of the European Regional Development Fund (ERDF) and the REACT-EU development aid. Within the scope of this project, an infrastructure for the large-area and flexible fabrication and characterization of a wide variety of nano structures in and on different substrates and materials is to be created in the clean rooms.



Research Association of the Institut für Mikroelektronik Stuttgart e.V.

The non-profit Research Association of the Institut für Mikroelektronik Stuttgart was established in 1983 and supports the contacts between industry and research. It is a contact point for talents from Germany as well as from abroad that will be supported by the IMS with a scholarship. It opens doors to member companies that sponsor them.

An annual member meeting takes place every year. Members receive a discount on trainings and events.

For further information, please refer to www.ims-forschungsverein.de.

Contact: Christina Ott • Pilz GmbH & Co. KG, Felix-Wankel-Straße 2, 73760 Ostfildern
Phone +49 711 3409-7949 • ims-forschungsverein@pilz.de